STAR R&D and Detector Upgrade

Howard Wieman
CCAST Workshop
11-Aug-2004
STAR Upgrade Projects

- MRPC TOF  Time of Flight
- HFT Heavy Flavor Tracker - Pixel micro-vertex
- Inner Tracker
- Forward Tracker
- DAQ1000
- FEE Upgrade
- Very Forward Cal
MRPC TOF  Time of Flight

- RPC high granularity high resolution TOF system
- Two following talks:
  - Hong-Fang Chen
  - Yi Wang
TOF
management chart
China STAR TOF construction project

**Project manager**
Y. Ma
SINAP

**Module production**
J. Cheng
Tsinghua

- Tsinghua production
  - Y. Li
  - Tsinghua
- USTC production
  - C. Li
  - USTC

**Quality control**
X. Wang
USTC

**Data analysis**
Y. Ma
SINAP

- Tsinghua QA
  - Y. Wang
  - Tsinghua
- USTC QA
  - X. Wang
  - USTC

**Test software**
M. Shao
USTC

- IOPP data analysis
  - F. Liu
  - IOPP
- USTC data analysis
  - J. Wu
  - USTC
- SINAP data analysis
  - Y. Ma
  - SINAP
MRPC R&D

Six cells
Cell area:
3.0cm × 6.0cm
Gas gap:
6 × 0.22mm
Timing
a) The raw time and
b) the T(A) corrected
time distributions.

Time resolution (σ)
before and after
quadratic subtraction
(scint. jitter ~ 30 ps)
Automated Fish Line Threader
MRPC Future Production Facility
TOF Development in the next run

- TOFp and CAMAC daq will be removed for Run 5
- Run 5 is an engineering run
- First HPTDC use
- First use of ALICE PCI-PC based DAQ
- New start detector for Run 6, possibly ready for part of Run 5
STAR HFT (Heavy Flavor Tracker), Micro Vertex Detector, Monolithic CMOS Detector

LBNL
Fred Bieser, Robin Gareus (Heidelberg), Leo Greiner, Howard Matis, Marcus Oldenburg, Fabrice Retiere, Kai Schweda, Hans-Georg Ritter, Eugene Yamamoto, Howard Wieman

LEPSI/IReS
Claude Colledani, Michel Pellicioli, Christian Olivetto, Christine Hu, Grzegorz Deptuch, Jerome Baudot, Fouad Rami, Wojciech, Dulinski, Marc Winter

UCI
Yandong Chen, Stuart Kleinfelder

BNL Instrumentation Div
Consulting

OSU
Ivan Kotov

Purdue
Dennis Reichhold
STAR Micro Vertex Detector

- **Two layers**
  - 1.5 cm radius
  - 4 cm radius

- **24 ladders**
  - 2 cm X 20 cm each
  - 30 µm X 30 µm pixels
  - ~ 100 Mega Pixels
  - < 0.2% $X_0$
  - 10 µm position resolution
Charm hadron reconstruction performances

(figure of merit)

<table>
<thead>
<tr>
<th>System</th>
<th>N events for 3 $\sigma$ $D^0$ signal</th>
<th>N events for 3 $\sigma$ $D^{+s}$ signal</th>
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<tbody>
<tr>
<td>TPC+SVT</td>
<td>12.6 M</td>
<td>In progress</td>
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<tr>
<td>TPC+SVT+TOF</td>
<td>2.6 M</td>
<td>$\sim$1,000 M ($\phi+\pi^+$)</td>
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<tr>
<td>TPC+SVT+$\mu$Vertex</td>
<td>100 K</td>
<td>$\sim$100 M ($\phi+\pi^+$)</td>
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<td>10 K</td>
<td>$\sim$1 M ($\phi+\pi^+$)</td>
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Sensors: Monolithic CMOS Active Pixel Sensors

- **Advantages**
  - Precise
  - Can be thin
  - Rather fast
  - Low power

- **Disadvantages**
  - Small signal
  - Not that fast
  - New
    - Need R&D
Monolithic CMOS detector, Active Pixel Sensor

- Electron hole pairs created in field free epi layer
- Diffusing electrons reflect off p boundary and collect on small n in p- epi diodes
- Collection time ~100ns
- Row and column selected with source follower readout
- Minimum size diodes for good charge to voltage gain and minimum noise \((1/C = 26 \mu V/e)\)
APS monolithic CMOS

- Active thickness 8 µm
- Most probable signal 450 e
- Noise ~17e, later development ~10e
- Fit with Bichsel calculation
MIMOSTAR LEPSI/IReS for first generation STAR detector

- Based on MIMOSA-5, full wafer engineering run - significant readout infrastructure on chip
- LBNL test board works (Bieser and Gareus)
  - 2 by 2 cm MIMOSA-5 chip
  - LBNL development using 4 commercial 50 MHz 14 bit ADCs
- MIMOSTAR Design
  - 1.9cmX1.9cm active
  - 30µmX30µm pixels
  - 409600 pixels/chip
  - Continuous frame read at 4-8ms per frame
  - 52 mW per chip
  - Analogue readout options
    - Single fast option 50 to 100 MHz
    - 10 at 10 MHz option
Inner vertex detector in STAR

New vertex detector centered in pointing detector, supported one end only

Conceptual design focused on rapid insertion and removal while preserving spatial mapping

End view showing 3 of 6 ladder modules
Support: Thin stiff ladder concept

- Under development
- Tested for thermal distortion
- Wind tunnel vibration tests

- 21.6 mm
- 254 mm

- aluminum kapton cable (100 µm)
- silicon chips (50 µm)
- carbon composite (75 µm)

Young’s modulus 3-4 times steel
TV Holography from ATLAS, LBNL

- Lucite wind tunnel
- Thin silicon ladder, tension support
- Laser light source
- Camera
Capacitive Probe Measurement of Ladder Displacement and Vibration

1.6 µm vibration

- Additional vibration measurements:
  High sensitivity accelerometer
  place of the STAR inner detector support structure
Next Generation Monolithic CMOS Detector R&D

- **Goal:** improve signal to noise and enable on chip zero suppression
- **Photo-gate technology**
  - Improve signal collection
  - On the fly CDS
- **On pixel clamp circuit for CDS**
- **Active reset to remove fixed pattern noise and reset KTC noise**
### Photo-gate geometry

- **Large photo-gate** to collect large fraction of the charge on a single pixel, directly on the p- epi layer
- **Small transfer gate** also directly on p- epi layer
- **Small drain (minimum capacitance)** connected to source follower gate (sense node)

**Photo-gate geometry**

- **Photo gate**
- **Transfer gate**
- **Drain**

**Materials**
- **SiO2**
- **Silicon**
- **Polysilicon**
- **Aluminum**
- **Conductor**

**Dimensions**
- **0.4 μm**
- **5 nm**
- **-2 μm**
- **1 μm**
- **1 μm**
- **20 μm**
- **8 μm**
- **x = 0.4 and 0.8 μm**

**Simulation quantities**
- **P epi 1.4x10^15 1/cm^3**
- **N+ 1x10^20 1/cm^3**

**Other layers**
- **Reset gate**
- **Sense node**
- **Drain**
- **Row select gate**
- **Source follower gate**
- **20 μm**
Photo-gate issues in standard CMOS

- No double poly process - possible poor transfer between gates because of low transverse field
- Floating n well between gates, a bad solution to the transfer problem with single poly
- Sub-micron process may solve problem
Photo gate/transfer gate operation (400 nm gap)

\[ V_{phg} = 0.8 \text{ V} \text{ transfer mode} \]

\[ V_{phg} = 2.4 \text{ V} \text{ collection mode} \]
Photo gate/transfer gate with 800 nm separation

- **Photo gate**
- **Trans gate**: 1.8 V
- **Drain**: 2.4 V

**V_{phg} = 0.8 V**
- Transfer mode

**V_{phg} = 2.4 V**
- Collection mode
First silicon tests, comparing photo-gate with standard diode structure

DC bias:
V photo-gate 0.6 V
V drain 2.4 V

Issue:
Why is the signal spread out – is it surface traps under the gate?
CDS clamp

- $kT$ noise removed by clamp circuit – noise scales as

$$\sqrt{\frac{kT}{C_2}}$$

Rather than

$$\sqrt{kTC_{\text{diode}}}$$
Active reset

- Signal from output is amplified to zero the input
- In test
Inner Tracker, associated R&D

Very Preliminary Design

MIT
Si-Tracker Very Rough Estimates I

- Barrel Geometry
  - Radius = 100, 150, 200 mm
  - Length = 240, 360, 480 mm
- Let's assume strip sensors:
  - Size = 40x40 mm^2
  - Pitch = 50 um => 768 channels per sensor
  - 16, 24, 32 ladders => 72 total
- For 3 stereo layers gives a total of:
  - 1392 sensors
  - 1,069,056 channels
- Comparable to PHOBOS if we take much simpler design into account
3GEM foil R&D work for Forward Tracker

N. Smirnov (Yale), D. Majka (Yale), C. Woody (BNL), H. Spinka (ANL), D. Underwood (ANL), M. Plesko (MIT-Bates), D. Hasell (MIT), Berndt Surrow (MIT)
Triple-GEM activities

- Outlook: Triple-GEM tile layout in GEANT (N. Smirnoff)

GEM foil size:
(10x10), (10x20), (30x30) cm²

strip pitch: 0.04 cm

Number of FEE channels: $1.3 \times 10^5$
Contact to TechEtch

- TechEtch GEM foil

Tech-Etch METALLURGY Report

CERN

Tech-Etch

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<td>holes/kapton</td>
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Tech-Etch, Inc.
45 Aldrin Road
Plymouth, MA 02360
(508) 747-0300
www.tech-etch.com
Goal of the prototype triple-GEM effort

- **Goal**
  - Design of at least three triple-GEM chambers to be installed and tested at STAR under beam conditions:
    - Establish collaboration to a US company to develop and manufacture GEM foils for applications in triple-GEM detectors and other applications such as GEM TPC readout schemes
    - Manufacture 2D-readout structures
    - Design of a flexible GEM chamber to install and replace GEM foils
    - Design of a chip readout system
  - **R&D team:**
    - Collaboration between STAR/PHENIX: ANL, BNL, MIT, Yale
  - **R&D and construction laboratory:**
    - In order to realize the design and construction of a GEM-type tracking detector for the RHIC collider experiments, a clean-room facility to handle, inspect and test GEM-foils besides the actual detector assembly is urgently needed
      - Strong interest by several MIT faculty and staff members to establish such a test and construction facility at LNS and MIT-Bates using two existing clean rooms setups used for the BLAST drift chamber construction
      - Minimal effort to re-use existing clean rooms for GEM applications
      - Profit from clean room experience at MIT Microsystems Technology Laboratory
      - Several clean room accessories are available for free from the MIT Microsystems Technology Laboratory based on industry donations (Contact to Dr. Vicky Diadiuk, Assistant Director, MIT Microsystems Technology Laboratory)
    - Other potential location: Yale
Readout of a triple-GEM chamber

- **Characteristics of the APV25-S1 readout chip**
  - First chip for a high energy physics experiment to exploit a modern commercial 0.25µm CMOS technology
  - Each chip contains 128 channels
  - Each channel consists of a preamplifier coupled to a shaping amplifier
  - The shaper output of each channel is sampled at 40MHz (LHC bunch crossing) into a 192 cell deep pipeline
  - The pipeline depth allows latency of up to 4µs, with 32 locations reserved for buffering events awaiting readout
  - Once a positive trigger signal arrives, the appropriate pipeline cells are marked and overwritten until the actual transfer out of the pipeline is complete
  - Each channel is read out by a circuit called APSP (Analogue Pulse Shape Processor) which can operate in two modes:
    - **Peak mode**: One sample per channel is read out from the pipeline (low data rate option)
    - **Deconvolution mode**: Three samples are sequentially read out and the output is a weighted sum of all three (high-date rate mode)
  - Last step: Output is sampled/held and fed to a multiplexer
  - Operating voltage: +/- 1.25V
  - Power consumption: 194mW/chip
  - On-board calibration circuits (charge injection) (gain: 1mA/MIP)
5000

DAQ1000 Developments

J. Landgraf, M. LeVine, T. Ljubicic
BNL
The New TPC Receiver Board Design

- The fiber link is the ALICE-developed “DDL”
  - 2.125 Gbaud optical link (effectively 50 MHz @ 32 bits on LVDS)
  - Bidirectional - will also be used to download pedestals, bad pads etc. to the FEEs
  - We can re-use many ALICE components/technologies on the FEE/RDO side

- The Receiver Board is a PCI board (certainly PCI 64/66, probably PCI-X, hopefully PCI-Express) - plugs in a fast/cheap PC with lots of fast/cheap memory & CPU power

- A board exists: ALICE D-RORC
  - 2 X 200 MB/s fiber on a PCI 64/66
  - Available! ($1500+)
  - Fully developed readout software (driver for Linux) the way we (mostly) like
  - NO cluster-finder in hardware - must be done in software on the PC host (see later)
  - Will be used for the new TOF DAQ (in progress)
  - A modified fiber (GLINK) daughtercard will be used as the new EMC PCI Receiver Board (under deliberation with Rice/TOF engineers)
Dual CERN D-RORC with fibers on the board

Pluggable Mezzanine DDL

Single D-RORC with 1 fiber mezzanine (we purchased 4)
STAR TPC FEE
Upgrade Status
6/2004

Fred Bieser
Was

- Analog store + digitize on FEE card
- Gather data, serialize, send to DAQ on RDO
- Subtract pedestals, suppress 0s in DAQ
Will Be

- Preamp/shaper (only) on FEE card
- Continuous waveform sampling, digital filtering, & zero suppression in ALTRO chip on RDO
- Format, serialize and send to DAQ on RCU card

preamp shaper  digitize adj. baseline  suppress 0s  serialize send to DAQ
ALICE TOPOLOGY

128 channels
Front End Card (FEC)

Capton Cable

140mm

190mm
STAR TOPOLOGY

- 32-channel PASA FEE cards
- RDO boards with 9 groups of 8 ALTROs acting as 9 ALICE FECs with ‘cable’ interconnects
- One ALICE RCU to control the ALTRO Bus and send data to DAQ via OPTO Link.
- 6 such RDOs per sector just as now.
A Forward Meson Spectrometer to Probe Gluon Distributions

FPD participants from UCB/SSL, BNL, Penn State, IHEP Protvino, UCLA, Argonne, TAMU
Motivation

- Detect $D^0 \rightarrow K^0\pi^0$ (BR=0.021), or $\pi^0\pi^0(0.008)$
  - $D^0$ mass = 1864 MeV, $\pi^0$ = 135 MeV, $K^0$= 498 MeV

- Compare $\pi^0$ and $D^0$ spectra at large $x_F(>0.3)$
  - from pp and dAu
  - $qg$ dominant process

- Do light and heavy quarks experience the same energy degradation in traversing the gluon field?

- Increase acceptance for $pp \rightarrow \pi^0 X$
FMS at STAR

~4 tons
Move pump

L.Bland
Forward Meson Spectrometer

~2.4m square

~1500 PMTs

3.8 cm inner
7.6 cm outer
In summary, STAR upgrade projects:

- MRPC TOF Time of Flight
- HFT Heavy Flavor Tracker - Pixel micro-vertex
- Inner Tracker
- Forward Tracker
- DAQ1000
- FEE Upgrade
- Very Forward Cal
Extend PID Capability to higher momentum

Using MRPC
**Electron Identification**

Before, using TPC dE/dx only to separate electrons from hadrons is complicated.

TOF detector lights up this study.

A prototype TOF tray (TOFr) installed last year.

\[ |1/\beta - 1| < 0.03 \]

With TOF PID cut, electron band can be separated from others easily!
Spacious electronic workshop
MRPC workshop > 200m²